DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Hartmann et al (US Patent 5,905,873).

Regarding to claims 1 and 9, Hartmann discloses a system 104 for integrated processing of different network protocols and multimedia traffics (fig. 1 col. 4 lines 53-65), comprising a common packet having a header and data to process multi-protocol (fig. 10 col. 14 lines 25-34); a common packet switch 570 for switching, bridging, and routing said common packet internally (fig. 6 col. 9 lines 48-63); a plurality of channels for exchanging said common packet through dedicated lines according to types of packets (fig. 7b col. 10 lines 52-60); a common bus 512 for transmitting said common packet to/from said common packet switch (fig. 5 col. 8 lines 22-34); a common protocol platform able to build free topology through an address translation so as to perform integrated processing of different protocols, different packet formats, and so on (fig. 7b col. 11 lines 19-29); an external network protocol converter 402 (fig. 8-9 col. 13 lines 43-

59) for converting a packet received from a wide area network into a common packet (col. 4 lines 54-65); and an internal network protocol converter (fig. 8-9 col. 13 lines 43-59) for converting a packet received from a local area network into a common packet (col. 4 lines 45-52).

Regarding to claims 2, 3, 11, and 12, Hartmann discloses a buffer part 254 storing temporarily an internal or external network packet entered (fig. 2 col. 6 lines 42-43); a conversion part 402 converting said internal network packet into said common packet (fig. 8-9 col. 13 lines 43-59); and a loader part loading 572 said common packet on said common bus to transmit said common packet to said common packet switch (fig. 6 col. 9 lines 53-61).

Regarding to claims 4 and 13, Hartmann discloses said common packet, said common bus, said common packet switch, said common packet platform, said external network protocol converter, and said internal network protocol converter are modularized so that each of them can be operated independently and they can interwork with one another (fig. 6 col. 9 lines 13-47).

Regarding to claims 5 and 14, Hartmann discloses said common packet, said common bus, said common packet switch, said common packet platform, said external network protocol converter, and said internal network protocol converter constitute a plurality of block combinations according to functions (fig. 6 col. 9 lines 13-47).

Regarding to claims 6 and 15, Hartmann discloses said common packet, said common bus, said common packet switch, said common packet platform, said external

network protocol converter, and said internal network protocol converter are integrated on a chip so that they can work as a single chip 112 (fig. 1 col. 4 lines 35-44).

Regarding to claims 7 and 16, Hartmann discloses in order to support a plug and play function said common packet, said common bus, said common packet switch, said common packet platform, said external network protocol converter, said internal network protocol converter are designed as an open architecture, and external networks or internal networks interwork with said common packet platform (col. 11 lines 19-29).

Regarding to claim 8, Hartmann discloses in addition to different network protocol conversions, an overlay function toward common packet is supported (col. 8 lines 45-56).

Regarding to claim 10, Hartmann discloses a buffer part 254 storing temporarily said common packet entered (fig. 2 col. 6 lines 42-43); a separate channel part based on types of traffic classes (fig. 7b col. 10 lines 52-60); a header conversion part 402 where a new destination address as desired is added to a header (fig. 8-10 col. 13 lines 43-59); and a loader part 572 loading existing data and said header with said new destination address on said common packet (fig. 6 col. 9 lines 53-61).

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Duong whose telephone number is (571)272-3122. The examiner can normally be reached on M-F (8:00 AM-5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wing Chan can be reached on 571-272-7493. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/D. T. D./
Examiner, Art Unit 2419

/Wing F. Chan/
Supervisory Patent Examiner, Art Unit 2619
10/25/08